AS210-04
DIGITAL DELAY GENERATOR MODULE

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PREFACE

This manual contains installation, operation and maintenance instructions for the AS210-04 Digital Delay Generator. The data contained herein is arranged as follows:

Reference Publications

AS210A-PM	Portable Mainframe Operation and Maintenance Manual
AS210RM, LM	Mainframe Operation and Maintenance Manual
AS210-01A	Module Controller Operation and Maintenance Manual
AS210-02	Frequency Comparator Operation and Maintenance Manual
AS210-03	Frequency Generator Operation and Maintenance Manual
AS210-05	Standby Battery Operation and Maintenance Manual
AS210-06	Microwave Generator Operation and Maintenance Manual
AS210-08	Distribution Amplifier Operation and Maintenance Manual
AS210-20	Time Clock Operation and Maintenance Manual

CHAPTER 1
GENERAL INFORMATION

1-1 INFORMATION

The AS210-04 Digital Delay Generator illustrated in Figure 1.1 is designed for installation in the ARGOSystems AS210 Electronic Frequency Counter and Frequency Standard Calibration System Mainframe. The Digital Delay Generator provides a means for generating a selectable, precise delay time between a reference pulse train and delayed pulse train. The reference pulses, delayed pulses and the time interval between them are derived from the Rubidium Frequency Standard in the Mainframe. The unit is programmable through an IEEE-488 interface located in the Module Controller. One application of the Digital Delay Generator is determination of performance characteristics of the time interval function of electronic counters.

1-2 PHYSICAL AND ELECTRICAL DESCRIPTION

The Digital Delay Generator consists of two circuit card assemblies and a front panel mounted in a modular type frame. Controls and connectors are on the front panel. Table 1-1 is an electrical specification for the AS210-04 Digital Delay Generator. Functionally the unit accepts a standard frequency input, converts the frequency and splits the signal into two channels, reference and delayed. The Pulse Repetition Frequency (PRF) of the pulse trains and the delay interval can be manually varied by an operator or controlled by a computer through the IEEE-488 bus.

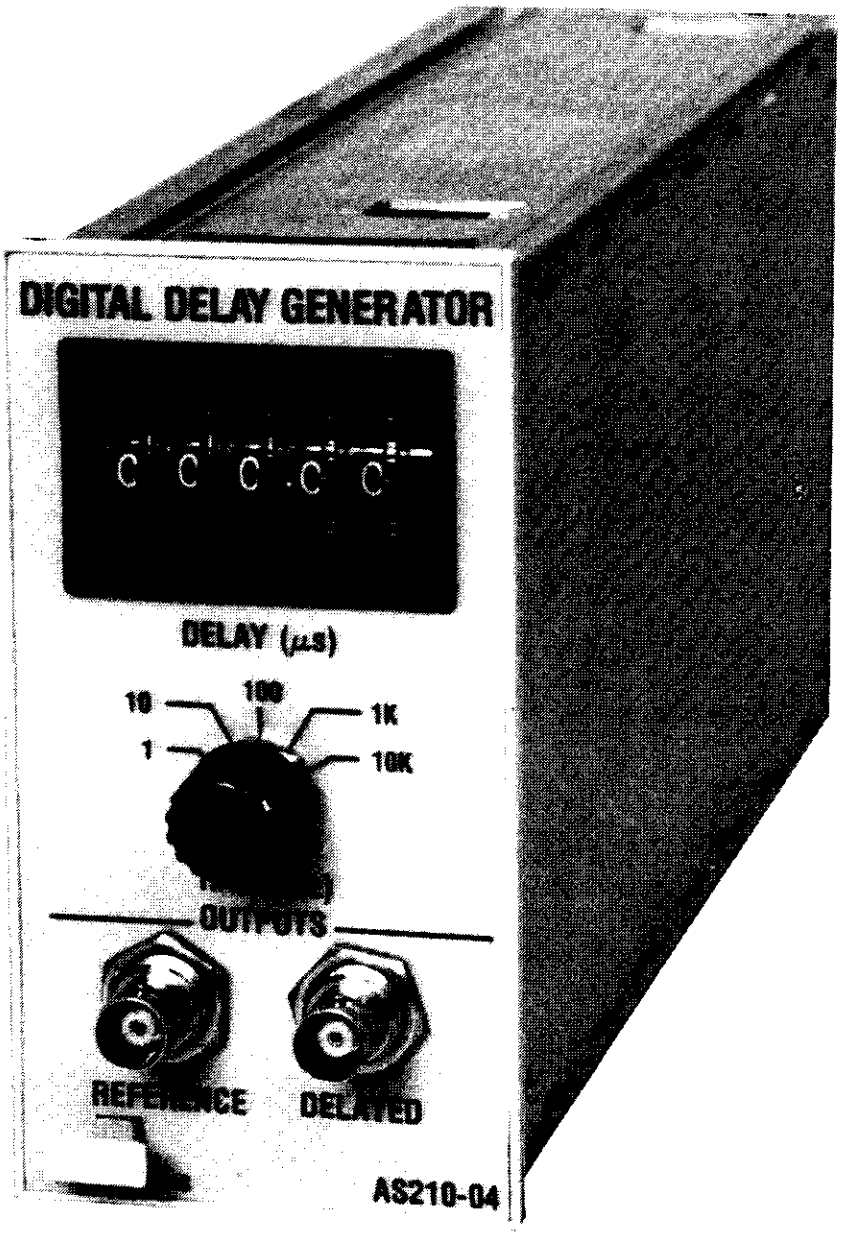

Figure 1.1 AS210-04 Digital Delay Generator

Table 1-1

AS210-04 EQUIPMENT SPECIFICATION

DELAY CHARACTERISTICS BETWEEN REFERENCE PULSE AND DELAYED PULSE	
RANGE	0-999.99 microseconds
RESOLUTION	10 nanoseconds
UNCERTAINTY	.01 - .09 microseconds delay ±1 nanosecond .1 - .99 microseconds delay ±2 nanoseconds 1.0 - 999.99 microseconds delay ±3 nanoseconds
REPEATABILITY	.01 - .99 microseconds ±0.2 nanoseconds maximum 1.0 - 999.9 microseconds ±0.6 nanoseconds maximum
OUTPUT PULSE CHARACTERISTICS WITH A 50 OHM TERMINATION	
	BNC connectors
OUTPUTS AVAILABLE	Referenced and delayed pulses; BNC connectors
TRANSITION TIMES	Less than or equal to 5 nanoseconds
PULSE WIDTH	10 microseconds nominal
LEVEL	-2.5 to +2.5 volts (5 VPP minimum)
PULSE REPETITION RATES	1, 10, 100, 1K or 10 KHz selectable
PHYSICAL CHARACTERISTICS	
OPERATING TEMPERATURE RANGE	0 to 40°C
POWER	Supplied by AS210 mainframe
SIZE	Single width plug-in
WEIGHT	2.25 pounds

CHAPTER 2
INSTALLATION

2-1 INTRODUCTION

The AS210-04 Digital Delay Generator module plugs into the AS210 Mainframe. The module is electrically connected through the rear connector and mechanically retained via a front panel locking bar on the mainframe. Power and singal interface is provided through the mainframe.

NOTE 1: Because of the high retention force of the rear card edge connector, it may be necessary to pull on the RATE control at the same time as the release mechanism is pulled to remove the Digital Delay Generator module from the mainframe.

NOTE 2: The power in the AS210 Mainframe must be turned off when inserting or removing the Digital Delay Generator.

CAUTION

AS210 series plug-ins will not work in Tektronix TM500 series mainframes. Severe damage will result if operation in this mode is attempted.

The signals are output through two BNC connectors. The cables should be equal length to avoid delay errors. There is a delay of approximately 1.5 nanoseconds/foot in RG58/U cable.

CHAPTER 3
OPERATION

3-1 INTRODUCTION

Operator interface with the AS210-04 Digital Delay Generator is provided through two controls and two connectors on the front panel of the module. The CPU interface is transparent to the operator. This chapter contains a front panel illustration keyed to a table explaining the function of the controls and connectors. The operating procedures provide applications and instructions for use of the Digital Delay Generator.

3-2 CONTROLS AND CONNECTORS

Figure 3.1 is a front panel photograph of the Digital Delay Generator with index numbers keyed to Table 3-1.

3-3 OPERATING INSTRUCTIONS

The AS210-04 is connected via 50 ohm cable with BNC connectors. See installation notes. Select the desired delay from 000.00 to 999.99 microseconds with the thumbwheel switch. Select the desired Pulse Repetition Frequency (PRF) of both outputs with the RATE switch.

NOTES

Maximum delay 98 microseconds on 10K Hz range

Maximum delay 998 microseconds on 1K Hz range

Fast rise-time may cause ringing on unterminated cable

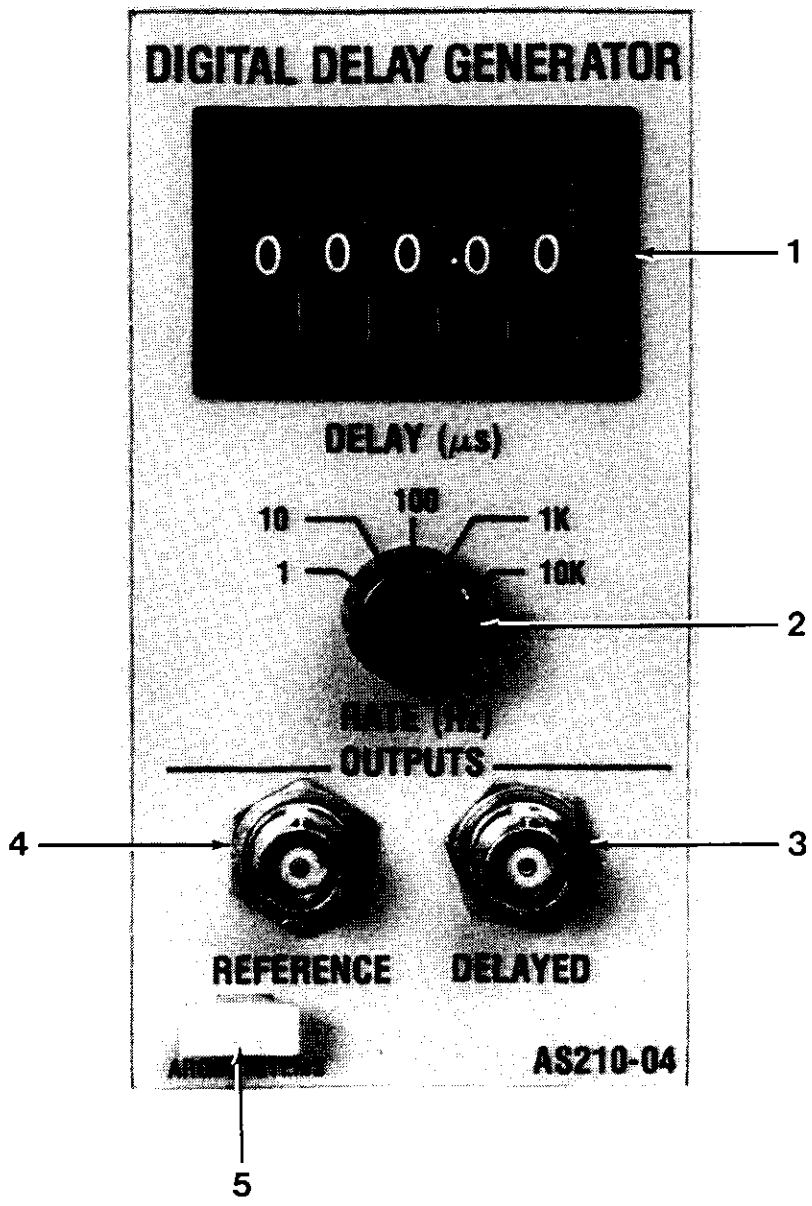

Figure 3.1 AS210-04 Front Panel Controls and Connectors

TABLE 3-1

AS210-04 FRONT PANEL CONTROLS AND CONNECTORS

INDEX NO. FIGURE 3-1	PANEL MARKING	FUNCTION
1	DELAY (microseconds)	Thumbwheel switch selects delay in microseconds between the REFERENCE pulse and DELAYED pulse outputs.
2	RATE (Hz)	Selects the pulse repetition frequency (PRF) of the output pulse signals.
3	DELAYED	The delayed pulse output. The PRF is selected by item 2, delay selected by item 1.
4	REFERENCE	The reference pulse output. The PRF is selected by item 2.
5	None	Release mechanism

CHAPTER 4
THEORY OF OPERATION

4-1 INTRODUCTION

This chapter provides an analysis of the circuits used in the Digital Delay Generator. The circuit descriptions are keyed to block diagrams, timing diagrams, and the schematic diagrams of the Maintenance chapter. Details of common circuits (power supplies, etc.) are not included in this description.

The main circuitry of the AS210-04 is contained on two circuit card assemblies designated A1 and A2. The Digital Delay Generator module receives a 10 MHz standard input signal from the Rubidium Frequency Standard on the AS210 Mainframe and produces two pulsed signal outputs. The PRF of the pulsed signals and the time delay between them are selectable. The AS210-04 is used in conjunction with the AS210-01 Module Controller which provides the CPU control and interface.

4-2 CLOCK CIRCUITS

The AS210-04 has a 100 MHz clock which is used for the timing and generation of the dual pulse trains (Figure 4.1). The 10 MHz standard input is divided by two at A1U12 to produce a 5 MHz reference input for phase detector A1U13. The phase detector output goes to loop amplifier/filter A1U14 providing the tuning voltage for the 100 MHz Voltage-Controlled Oscillator (VCO) A1Q2 and A1Q3. The 100 MHz signal is divided by 20 at A1U19 and A1U20 then applied to the variable input of A1U13. The VCO is thus phase locked to the 10 MHz frequency standard. One output of the VCO is sent to driver A1U21 which translates the signal to ECL levels needed for the delay producing circuits. The second output of the VCO is divided by 10 at A1U20,

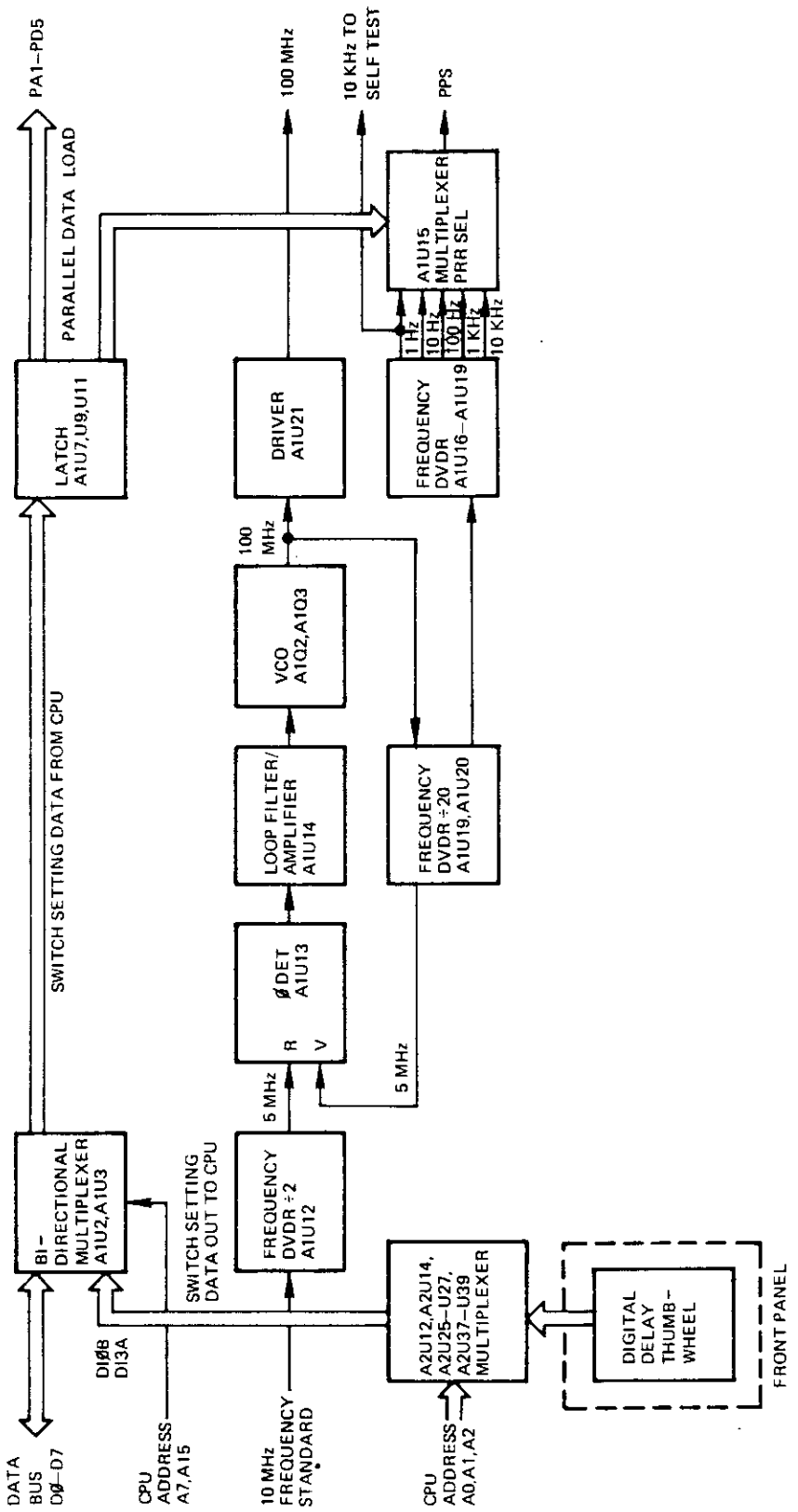

Figure 4.1 Data Interface and Clock Circuits

converted to TTL at A1Q4 and applied to the frequency-division circuit consisting of A1U16, A1U17, A1U18, and A1U19. Signals of 1 Hz, 10 Hz, 100 Hz, 1 KHz and 10 KHz are produced by this division circuit and applied to PRF select multiplexer A1U15. The multiplexer is addressed by the CPU which scans bidirectional multiplexer A1U2 and A1U3 ten times per second to determine the status of the front panel RATE and Delay switches. The 100 MHz clock, 10 KHz clock and one of the five PPS outputs (selected via A1U15) are sent to the timing and reference circuits.

4-3 DATA INTERFACING CIRCUITS

The RATE switch and DELAY thumbwheel switches are connected to the CPU data bus via multiplexers A2U12, A2U14, A2U25-U27 and A2U37-U39 (Figure 4.1). The 8-bit data bus (D11A-D13B) connects to a bidirectional multiplexer A1U2 and A1U3 which is addressed by the CPU (address bits A7, A15) and controlled by the $\overline{RD}$ signal from the CPU. Counters A2U31-U34 and A2U20 (Figure 4.2) are loaded with data from the DELAY thumbwheel as follows. The BCD thumbwheel data is applied to the multiplexer addressed by the CPU as described above. This data is sent over the data bus and returned under program control to be latched into A1U7, A1U9 and A1U11 (Figure 4.1). When these latches are appropriately addressed by the CPU their data is loaded into the counters.

4-4 REFERENCE PULSE AND DELAYED PULSE GENERATION CIRCUITS

The product of the Digital Delay Generator is two pulse trains at a selected PRF (RATE) and selected time delay between pulse trains. Refer to Figure 4.2 throughout the following discussion. The significant signals, developed by previously described circuits, are the 100 MHz phase locked clock signal, the selected rate (PPS) and the delay data dialed by the operator into the thumbwheels and returned to the unit via the CPU data bus. Four bits of the delay data (PA1-PD1) are loaded into ÷10 counter A2U20. This is a high speed ECL counter and the data is converted to ECL levels prior to loading in A2U20. The 100 MHz clock signal is also converted to ECL and applied to the counter's clock input. The $\overline{Q0}$ and $\overline{Q8}$ output of A2U20 are

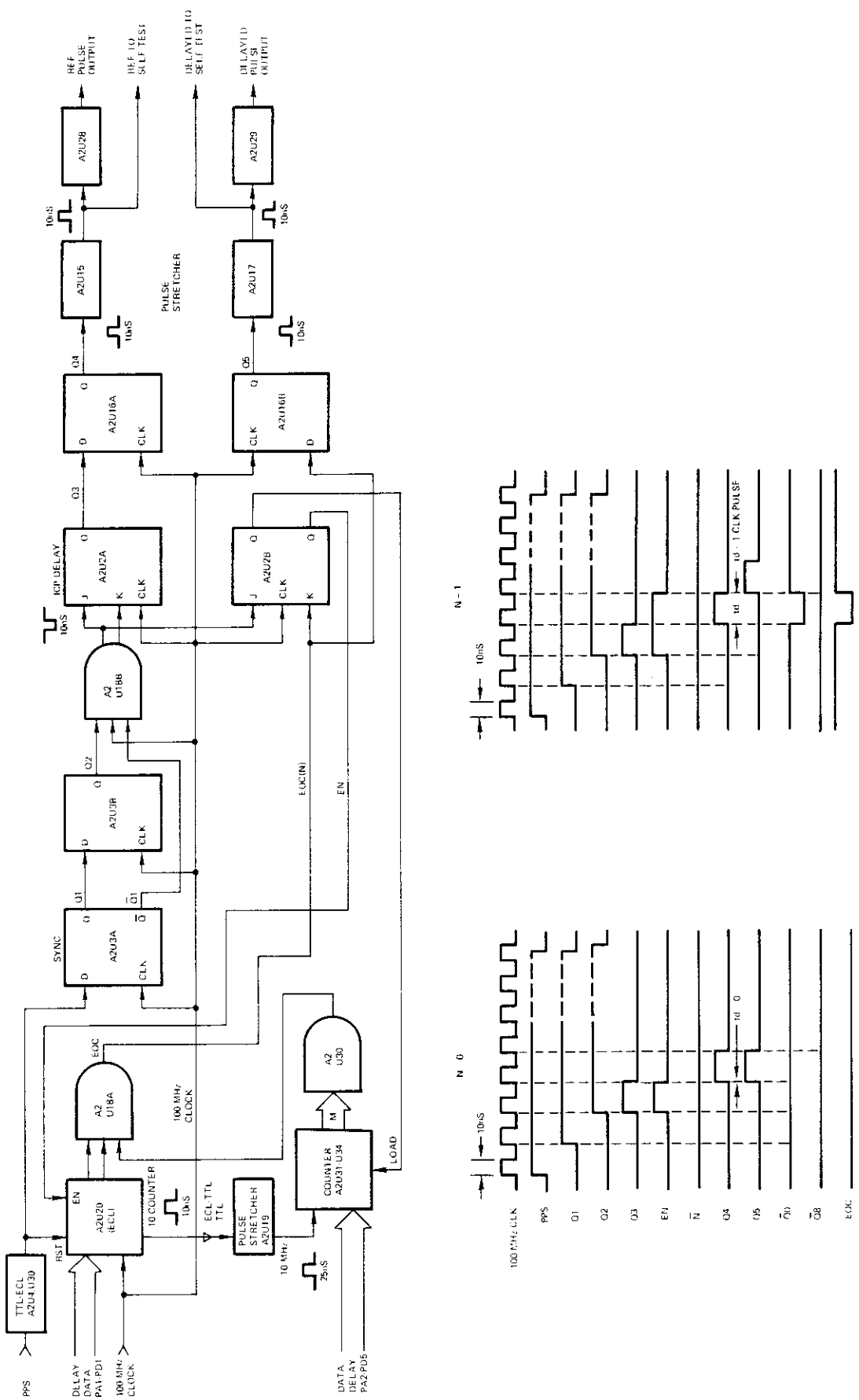

Figure 4.2 Reference and Delay Pulse Generator Circuit Diagram and Timing Diagram

applied to gate A2U18A. The 100 MHz clock is divided by 10 to 10 MHz by A2U20. The 10 MHz pulses are stretched to 25 nanoseconds by one-shot A2U19 and applied to the clock input of ripple counters A2U31-U34. The counters are preloaded with the remaining lines of the data bus (PA2-PD5) containing delay data. As each of these counters reaches zero from its preloaded number, the M/N (minimum/maximum) output is applied to gate A2U30. The output of A2U30 goes low when counters A2U31-U34 have reached the end of their count and is applied to A2U18A with $\overline{Q0}$ and $\overline{Q8}$ from A2U20. The output of A2U18A (EOC) is applied to the K input of A2U2B. The PPS signal is synchronized with the 100 MHz clock by A2U3A. The output of A2U3A (Q1) is applied to the D input of A2U3B with the 100 MHz clock at its CLK input. Signal Q2 is therefore delayed from Q1 by 1 clock pulse. Q2, the 100 MHz clock, and $\overline{Q1}$ are applied to gate A2U18B which goes high 1 clock period behind the PPS signal. The false output of A2U18B is applied to the K input of A2U2A while the true output is applied to the J input of both A2U2A and A2U2B. The 100 MHz clock drives both A2U2A and A2U2B while the EOC signal is applied to the K input of A2U2B. The Q3 signal from the output of A2U2A is delayed from signal Q2 by one 10 nanosecond clock period. The Q output of A2U2B is the load enable (EN) for counters A2U31-U34 while the $\overline{Q}$ output enables counter A2U20. A2U16A and U16B are both clocked by the 100 MHz clock signal. Q3 is the D input of A2U16A and the EOC signal is the D input of A2U16B. The EOC pulse is one clock period wide (10 nanoseconds) and is delayed N clock pulses from Q3. The output of A2U16A (Q4) is a reference pulse train synchronized with the 100 MHz clock while the output of A2U16B (Q5) is a pulse train delayed by the number of clock periods represented in the length of the EN pulse. Both pulse trains are pulse stretched to 10 microseconds by A2U15 and A2U17. A2U28 and A2U29 are current drivers for both outputs.

4-5 SELF-TEST CIRCUITS

The self-test circuits are illustrated in Figure 4.3. The inputs to this circuit are the 100 MHz clock, reference pulse train, delayed pulse train and a 10 KHz clock developed in the timing circuits. The purpose of the self-test function is to ensure that the actual pulse delay equals the

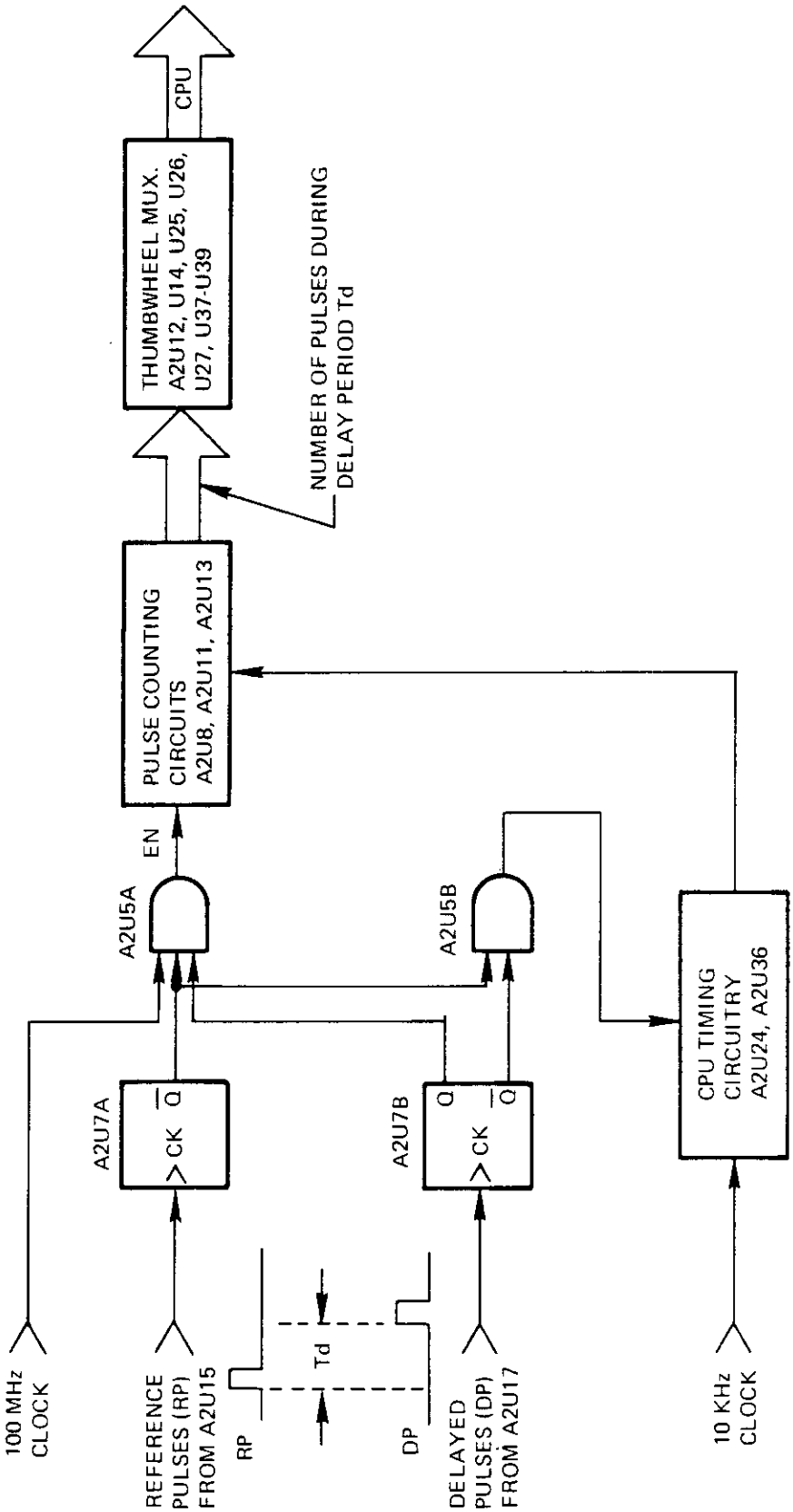

Figure 4.3 Self-Test Circuit

dialed-in thumbwheel setting. Reference pulses from A2U15 and delayed pulses from A2U17 are applied to the D input of A2U7B and A2U7A respectively. The 100 MHz clock signal is applied to the clock inputs of both flip-flops simultaneously. The DP output from A2U7B is thus delayed from the RP output of A2U7A by a time equal to the programmed delay time between the two pulse trains. When these two signals (RP and DP) are input to gate A2U15 with the 100 MHz clock the output is a pulse (EN) whose duration equals the time delay Td. The EN signal is applied to the enable input of pulse counter A2U8 which is driven by the 100 MHz clock. The output of A2U8 represents the number of 100 MHz pulses counted during the delay period Td. This count, accumulated by A2U8, A2U11 and A2U13, goes to thumbwheel multiplexers A2U12, A2U14, A2U25, A2U26, A2U27, A2U37, A2U38, A2U39 where it is scanned by the CPU. The CPU is also scanning the thumbwheel settings as part of the normal program and makes a comparison between the two readings. An error determination is displayed as a fault on the module controller's display unit.

CHAPTER 5
MAINTENANCE AND CALIBRATION

5-1 INTRODUCTION

The purpose of this chapter is to provide maintenance and calibration data for the AS210-04 Digital Delay Generator. Section I covers routine preventative maintenance procedures. Section II outlines performance tests for the Digital Delay Generator. Section III contains the calibration/alignment procedures for the AS210-04 module, and Section IV describes troubleshooting data. Figures 5.4 and 5.5 are the schematic diagrams for the Digital Delay Generator. The two truth tables on Figure 5.5 are for the Thumbwheel switch and RATE switch. For example, if the thumbwheel switch is set at 300.00 microseconds and the RATE switch is set at 1 KHz then input lines A5 on A2U27, B5 on A2U37, RA on A2U12, RB on A2U14, and RC on A2U26 will float high. All other input lines will be low. Please contact the factory for any assistance required in the maintenance or servicing of the AS210-04.

SECTION I

5-2 PREVENTIVE MAINTENANCE

Table 5-1 lists preventive maintenance checks and services which should be performed regularly.

TABLE 5-1

PREVENTIVE MAINTENANCE CHECKS AND SERVICES

ITEM	PROCEDURES
CABLES	Visually inspect cables for strained, cut frayed, or other damaged insulation.
CLEANLINESS	Make sure the exterior surfaces of the unit are clean. If necessary, clean exterior surfacs as follows: A. Remove the dust and loose dirt with a clean soft cloth. B. Remove dust or dirt from plugs and jacks with a brush. WARNING Use only warm soapy water for cleaning all plastic parts. Many solvents will cause the plastic to become brittle.
CORROSION	Make sure exterior surfaces of unit are free of rust and corrosion.
PRESERVATION	Inspect exterior surfaces of the unit for chipped paint or corrosion. If necessary, spot-paint surfaces as follows: A. Remove rust and corrosion from metal surfaces by lightly sanding them with sandpaper. B. Brush two coats of paint on base metal to protect it from further corrosion.

SECTION II

5-3 PERFORMANCE TESTING

This section describes the procedure to test the AS210-04 Digital Delay Generator to assure proper performance of the instrument. The AS210-04 must be used in conjunction with the AS210-01 Module Controller since the CPU in the AS210-01 monitors the controls and output of the AS210-04. The AS210-04 Digital Delay Generator will not operate without the AS210-01 Module Controller installed. If the AS210-04 fails any of the performance tests, please see Section III, Calibration/Alignment procedures, and/or Section IV, Troubleshooting procedures in this chapter.

5-4 AS210-04 TIME INTERVAL PERFORMANCE TEST

The following is a procedure for testing the time interval between the reference and delayed output pulse trains of the AS210-04 Digital Delay Generator. Table 5-2 contains the required equipment to perform this test.

Table 5-2

REQUIRED TEST EQUIPMENT FOR THE TIME INTERVAL PERFORMANCE TEST OF THE AS210-04

ITEM	RECOMMENDED TEST EQUIPMENT
ELECTRONIC COUNTER	Hewlett-Packard 545A
FREQUENCY STANDARD	Hewlett-Packard 5061A or 5062C Opt 01
COAXIAL CABLE (3 required)	3 Foot Long, 50 Ohm, BNC

5-5 TEST PROCEDURE

A. Ensure that power is disconnected from the AS210 system before beginning this procedure.

B. Connect the equipment as indicated in Figure 5.1 and apply power to the AS210. The Rubidium Frequency Standard in the AS210 system will require 20 minutes warm-up time to reach the specified frequency accuracy.

C. Set the electronic counter controls to measure time interval, with 50 Ohm input impedance and external time base.

D. Set the AS210-04 Digital Delay Generator to each position listed in Table 5-3. At each setting, verify that the electronic counter indication is within the tolerance limits listed. If any of the indications fall out of the limits for acceptable performance, please see Section III, Calibration/ Alignment Procedures, and/or Section IV, Troubleshooting Procedures.

E. Disconnect the frequency counter from the AS210-04.

5-6 AS210-04 REFERENCE AND DELAYED OUTPUT PULSEWIDTHS PERFORMANCE TESTS

The following is a procedure for testing the reference and delayed output pulse widths of the AS210-04 Digital Delay Generator. Table 5-4 on page 5-7 contains the required equipment for this performance test.

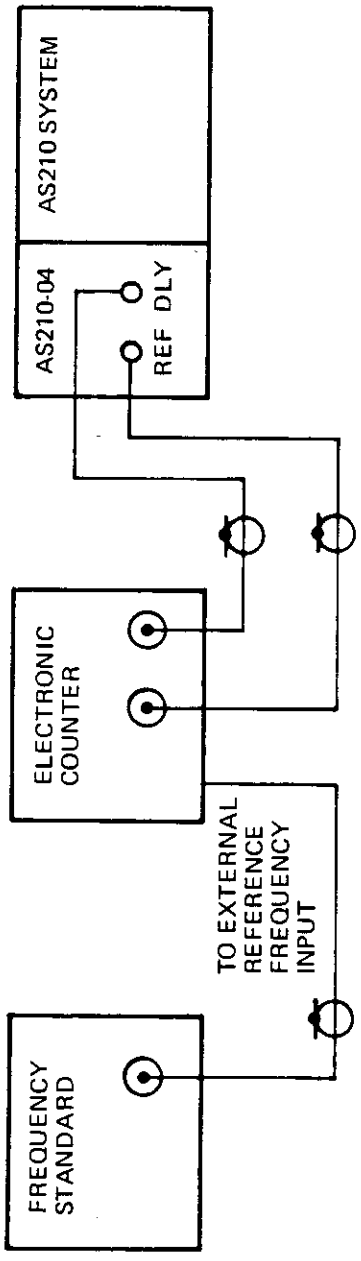

Figure 5.1 Test Configuration for Time Interval Performance Test of the AS210-04

TABLE 5-3

AS210-04 DIGITAL DELAY GENERATOR SWITCH SETTINGS AND CORRESPONDING TIME INTERVAL TOLERANCE LIMITS

DELAY SWITCHES (microseconds)	RATE OUTPUTS SWITCH (Hz)	ELECTRONIC COUNTER TOLERANCE LIMITS
000.02	10K	19 to 21 nanoseconds
000.13	10K	128 to 132 nanoseconds
004.44	10K	4.437 to 4.443 microseconds
055.55	10K	55.547 to 55.553 microseconds
066.66	1K	66.657 to 66.663 microseconds
077.77	1K	77.767 to 77.773 microseconds
088.88	1K	88.877 to 88.883 microseconds
111.11	1K	111.107 to 111.113 microseconds
999.99	100	999.987 to 999.993 microseconds
44.44	100	44.437 to 44.443 microseconds
33.33	100	33.327 to 3.333 microseconds
222.22	100	222.217 to 222.223 microseconds
222.22	10	222.217 to 222.223 microseconds
22.22	10	22.217 to 22.233 microseconds
111.11	10	111.107 to 111.113 microseconds
900.00	10	899.987 to 900.003 microseconds
999.99	1	999.987 to 999.993 microseconds
987.65	1	987.647 to 987.603 microseconds
876.10	1	876.097 to 876.103 microseconds
050.10	1	50.097 to 50.103 microseconds

TABLE 5-4

REQUIRED TEST EQUIPMENT FOR REFERENCE AND DELAYED OUTPUT PULSEWIDTHS OF THE AS210-04

ITEM	RECOMMENDED TEST EQUIPMENT
OSCILLOSCOPE WITH PROBES	Tektronix 465 or Equivalent
COAXIAL CABLE (2 required)	3 Foot Long, 50 Ohm, BNC

5-7 TEST PROCEDURE

A. Ensure that power is disconnected from the AS210 system before beginning this procedure.

B. Connect the equipment as indicated in Figure 5.2 and apply power. The Rubidium Frequency Standard in the AS210 system will require 20 minutes warm-up time to reach the specified frequency accuracy.

C. With an oscilloscope, monitor the reference and delayed output pulse trains at the front panel of the AS210-04. Both the reference and delayed output pulses should be between 9 and 11 microseconds wide. If the output pulses are out of this tolerance then consult Section III, Calibration/Alignment Procedures, and/or Section IV, Troubleshooting Procedures.

D. Disconnect the oscilloscope from the AS210-04 output connectors.

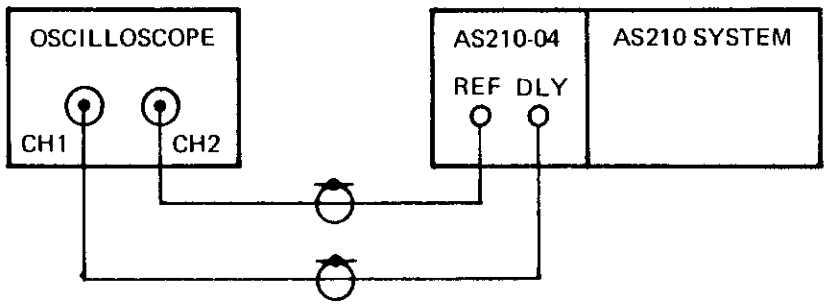

Figure 5.2 Test Configuration for Reference and Delayed Output Pulsewidth Performance Test of the AS210-04

SECTION III

5-8 CALIBRATION/ALIGNMENT PROCEDURE

WARNING

The following Calibration/Alignment Procedures (Chapter 5, Section III) and Troubleshooting Procedures (Chapter 5, Section IV) are for use by qualified personnel only. To avoid personal injury, do not perform any servicing other than that of Routine Maintenance (Chapter 5, Section I) and Performance Testing (Chapter 5, Section II) unless you are qualified to do so.

Figure 5.3 is a flow diagram of the Calibration/Alignment Procedure for the AS210-04 Digital Delay Generator. Use this flow diagram with the theory of operation in Chapter 4, the text in this chapter, and the illustrated parts lists in Chapter 6. The AS210 internal frequency standard calibration data, contained in the AS210 mainframe operation and maintenance manual, is also referenced in this flow diagram. Please note that it is not necessary to diassemble the AS210 system to determine if calibration/alignment is needed. For any assistance needed in performing this calibration/alignment procedure, please contact the factory.

5-9 ACCESS TO AS210-04 DIGITAL DELAY GENERATOR MODULE

Please reference the AS210 mainframe manual for the disassembly procedure of the AS210 system to allow access to the AS210-04 Digital Delay Generator module. Access to the module circuitry itself is gained by removing the two metal side covers with a small straight-blade screwdriver. Place the module on one of its sides so that one cover is facing up. Starting with the end toward the edge connector, insert the screwdriver into one of the slots where the cover mates with the module chassis and pry the cover up. It will be necessary to move along the slot toward the front panel of the module

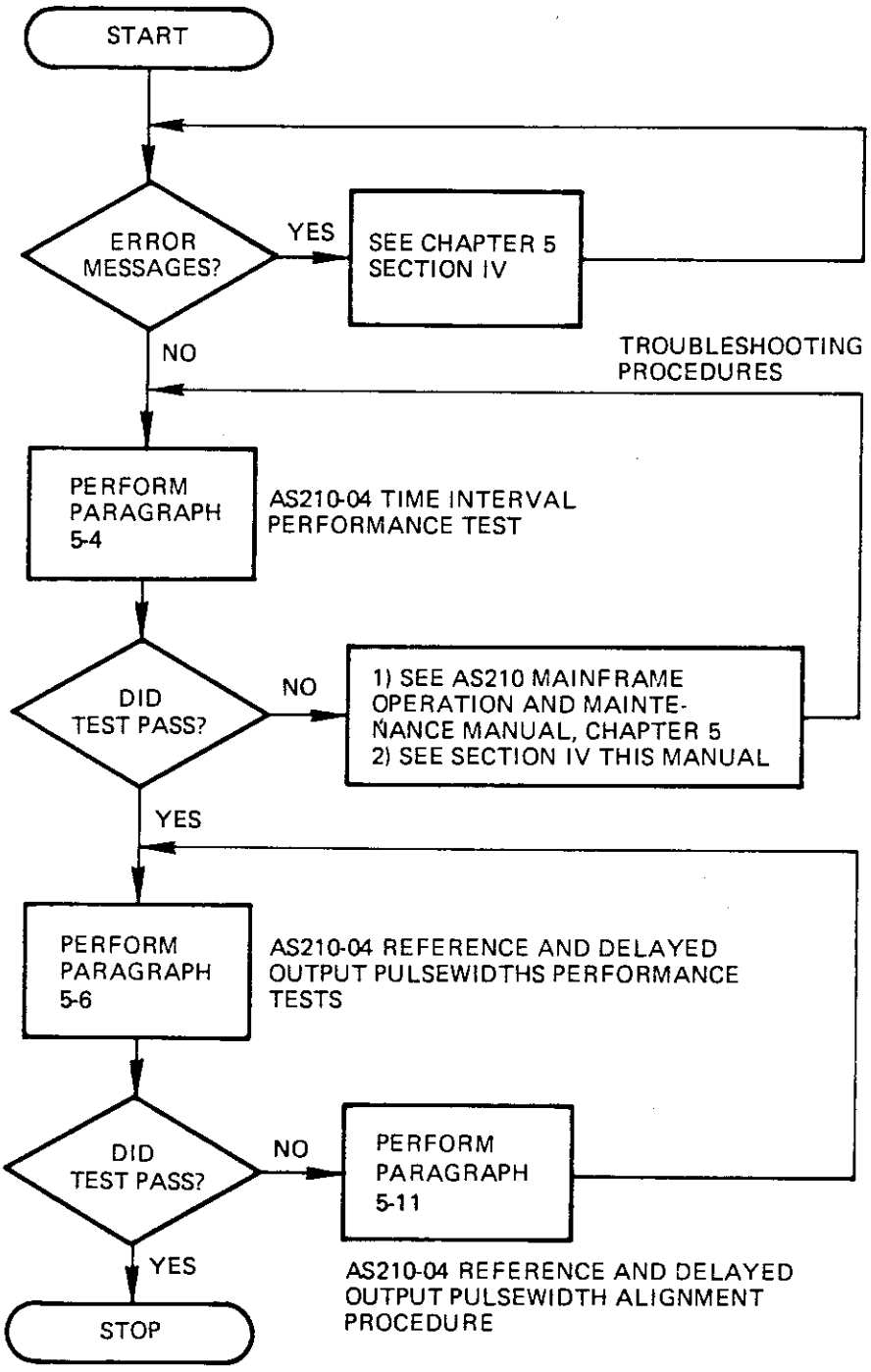

Figure 5.3 Flow Diagram of the Calibration/Alignment Procedure for the AS210-04 Digital Delay Generator

and repeat the prying action to loosen the side of the cover from the module. Repeat this technique to free the other side of the cover from the chassis. Set the free cover clear of the module and flip the module over so that the second cover is now facing up. Repeat the above procedure to free this cover.

5-10 PLO ALIGNMENT PROCEDURE

The following is the alignment procedure for the phase-locked oscillator (PLO) in the AS210-04 Digital Delay Generator. Table 5-5 contains the required test equipment for this alignment procedure.

TABLE 5-5
REQUIRED TEST EQUIPMENT FOR THE PLO ALIGNMENT PROCEDURE

ITEM	RECOMMENDED TEST EQUIPMENT
OSCILLOSCOPE WITH PROBES	Tektronix 465 or Equivalent
ELECTRONIC COUNTER	Hewlett-Packard 5345A
COAXIAL CABLE	3 Foot Long, 50 Ohm, BNC

A. Obtain access to the AS210-04 module circuits by referencing paragraph 5-9 in this chapter.

B. Using the oscilloscope monitor the voltage level on pin six of U14 located on assembly A1 (117241).

C. Adjust the variable capacitor A1C3 in a clock-wise direction until a level of -4VDC is obtained.

The AS210-04 Digital Delay Generator output frequencies should now be aligned. To confirm that the digital delay generator is operating

properly, reference Section II, Performance Testing of the AS210-04 contained in this chapter.

5-11 AS210-04 REFERENCE AND DELAYED OUTPUT PULSE WIDTH ALIGNMENT PROCEDURE

The following is the alignment procedure for the referenced and delayed output pulse widths of the AS210-04. Table 5-6 contains the required test equipment for the alignment procedure.

Table 5-6

REQUIRED TEST EQUIPMENT FOR THE AS210-04 REFERENCE AND DELAYED OUTPUT PULSE WIDTH ALIGNMENT PROCEDURE

ITEM	RECOMMENDED TEST EQUIPMENT
OSCILLOSOPE WITH PROBES	Tektronix 465 or Equivalent
COAXIAL CABLE (2 Required)	3 Foot Long, 50 Ohm, BNC

A. Obtain access to the AS210-04 Digital Delay Generator module circuits by referencing paragraph 5-9 in this chapter.

B. Monitor the reference and delayed output pulse widths of the AS210-04 with the oscilloscope as in Figure 5.2.

C. Adjust R17 and R23 for the reference and delayed nominal output pulse widths of 10 microseconds.

The AS210-04 Digital Delay Generator output levels should now be aligned. To confirm that the Digital Delay Generator is operating properly, reference Section II, Performance Testing of the AS210-04, contained in this chapter.

SECTION IV

5-12 TROUBLESHOOTING PROCEDURES

Troubleshooting of the Digital Delay Generator is facilitated by a combination of error codes displayed on the module controller display and LED indicators on the circuit card assembly, A1. The circuit cards A1 and A2 are illustrated in Figure 6.1. Table 5-7 correlates the error code, displayed on the module controller when a fault occurs, to the malfunction. An explanation of the problem is provided with possible solutions. Table 5-8 is a list of visual indicators on circuit card A1 and the meaning of their indications. For further assistance, please contact the factory.

Table 5-7
ERROR CODE LISTING

ERROR CODE	PROBLEM	RECOMMENDED SOLUTION
4-00	On 10 KHz setting delay >99 microseconds or on 1 KHz setting delay >999 microseconds	Reduce delay setting or repetition rate.
4-20 to 4-22	Self-test delay error 20 = 1 Hz 21 = 10 Hz 22 = 100 Hz	Check delay generator circuit.
4-10 to 4-12	Self-test, PRR not equal to 1 pps, 10 pps or 100.	Check repetition rate circuit (see Table 5-2).
4-30	Self-test delayed pulse not occurring.	Self-test circuit failed. Repetition rate generator failed.

Table 5-8

VISUAL INDICATORS

INDICATOR		
A1CR1, CR2 OFF	10 MHz Reference Signal Failure	Check 10 MHz Reference Input, A1Q1, U12.
A1CR3, CR4 OFF	Oscillator	Check A1Q2, Q3, U20, U21, Q4, U19 or U12.
A1CR5 ON	100 MHz Oscillator in Unlock Condition	If CR1-CR4 are OK, check A1U13, U14.

CHAPTER 6
ILLUSTRATED PARTS LIST

6-1 INTRODUCTION

This chapter contains an illustrated parts list for the Digital Delay Generator Module. The assembly numbers and assembly title are listed at the top of the parts lists. The parts lists are divided into six columns and arranged in the following order:

Column 1 - Item Number

Column 2 - Quantity per assembly.

Column 3 - Manufacturer's Code

Column 4 - Part Number

Column 5 - Description

Column 6 - Reference Designation

ASSEMBLY NUMBER 117171-01 - DIGITAL DELAY GENERATOR AS210-04

ITEM	QTY	MANUFACTURER'S CODE	PART NUMBER	DESCRIPTION	REF. DESIG.
1	1	33472	117240-01	Digital Delay Generator Assembly	A1
2	1	33472	117245-01	Digital Delay Generator Assembly	A2
3	0	33472	117326	Frame Section Modification	
4	1	33472	117350-03	Cable Assembly Ribbon, 50 Wire	
5	1	33472	117357-02	Cable Assembly Coax	
6	4	06540	8225-SS-0632	Standoff, 6-32x1&5/16" Threaded	
7	8	81349	MS51957-27	Screw, PNH 6-32 x 5/16	
8	8	81349	NAS620-C6	Reduced OD Flat Washer #6	
9	8	81349	MS35338-136	Split Lock Washer #6	
10	1	33472	117183-01	Panel, Lexan	
11	1	33472	117183-02	Subpanel, Plastic	
12	1	33472	117183-03	Panel, Rear	
13	1	95146	PKG-50B 1/4	Knob, Black	
14	1	33472	117347-01	Harness Assembly	
15	1	33472	117356-02	Cable, Coaxial	
16	1	33472	117356-03	Cable, Coaxial	
17	1	80009	366-1690-10	Latch Pull	
18	1	80009	105-0718-01	Latch	
19	1	80009	426-0724-00	Bottom	
20	2	80009	337-1399-00	Side Cover	

ASSEMBLY NUMBER 117171-01 - DIGITAL DELAY GENERATOR AS210-04 (Continued)

ITEM	QTY	MANUFAC-TURER'S CODE	PART NUMBER	DESCRIPTION	REF. DESIG.
21	1	80009	214-1061-00	Tension Spring	
22	1	80009	426-0725-00	Top	
23	2	80009	386-3657-01	Guide Pin	
24	1	81349	00000	Screw FLH STL Sheet Metal #2X1/4	
25	4	81349	MS24693-C26	Screw 6-32X3/8 FLH	
26	4	81349	00000	Screw PNH STL Sheet Metal #6X3/8	

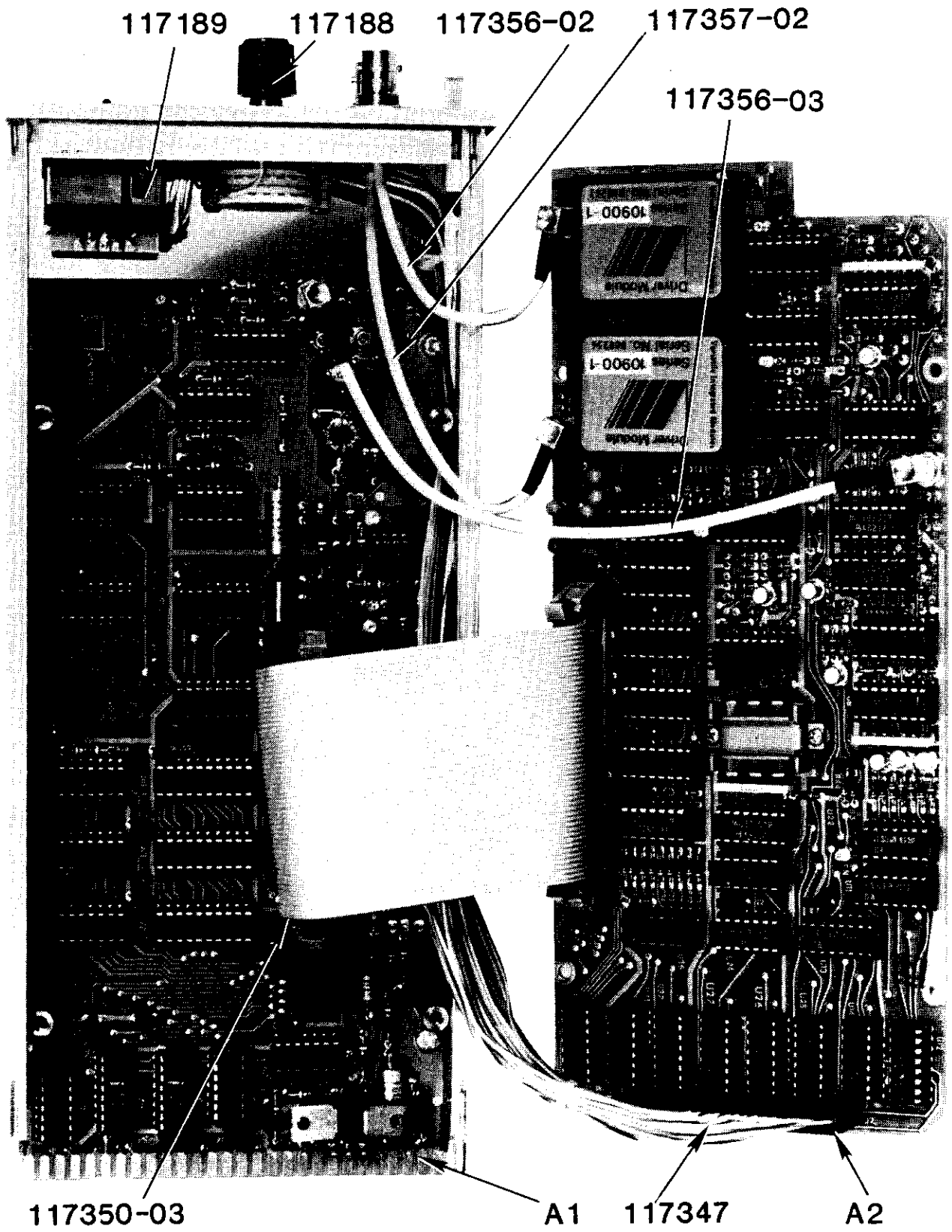

Figure 6.1 AS210-04 Digital Delay Generator

ASSEMBLY NUMBER 117240-01 - DIGITAL DELAY GENERATOR A1

ITEM	QTY	MANUFAC-TURER'S CODE	PART NUMBER	DESCRIPTION	REF. DESIG.
1	1	33472	117243	PWB	
2	0	33472	117241	Schematic	
3	0	33472	117240	Assembly Drawing	
4	1	81349	CKO5BX103K	.01 UFD 10% Ceramic Capacitor	C9
5	17	81349	CKO5BX104K	.1 UFD 10% Ceramic Capacitor	C10,C12,C14, C20-27, C30-32, C34-36
6	2	51642	300-50-601-105M	1 UFD 20% Ceramic Capacitor	C13,C18
7	2	81349	CKO5BX471K	470 PFD 10% Ceramic Capacitor	C6,C7
8	1	81349	CKO5BX473K	.047 UFD 10% Ceramic Capacitor	C16
9	1	81349	CKO5BX102K	.001 UFD 10% Ceramic Capacitor	C33
10	1	81349	CKO5BX472K	.0047 UFD 10% Ceramic Capacitor	C37
11	3	81349	CKO5BX101K	100 PF 10% Ceramic Capacitor	C38,C39,C40
12	2	81349	100-100-COG689J	6.8 PFD 5% Ceramic Capacitor	C4,C5
13	1	72982	513-010-A2-10	2-10 PFD Variable Capacitor	C3
14	3	56289	CSR13G106KL	10 UFD, 50V, Electrolytic Cap	C8,C15,C19
15	4	15849	2010B-1	Terminal	
16	2	04713	MV2203	Tuning Diode	CR6,CR7

ASSEMBLY NUMBER 117240-01 - DIGITAL DELAY GENERATOR A1 (Continued)

ITEM	QTY	MANUFAC-TURER'S CODE	PART NUMBER	DESCRIPTION	REF. DESIG.
17	5	50434	5082-4487	Light Emitting Diode	CR1-CR5
18	1	53387	3433-2202	50 Pin PC Mount Male Header	J3
19	1	98291	51-051-0000	Snap On Conhex Connector	J4
20	2	99800	1025-48	15 UHY Molded RF Choke	L1,L4
21	1	33472	117305-05	Center Tapped Inductor	L2
22	1	02114	VK200-20/4B	Wide Band Choke	L3
23	2	04713	2N5179	NPN Transistor	Q2,Q3
24	1	27014	2N2222A	NPN Transistor	Q1
25	1	04713	MPS3639	PNP Transitor	Q4
26	2	81349	RCR07G151JS	150 ohm 5% 1/4W Carbon Comp	R6,R18
27	4	81349	RCR07G102JS	1K 5% 1/4W Carbon Comp	R20,R22,R25, R36
28	1	81349	RCR07G103JS	10K 5% 1/4W Carbon Comp	R24
29	1	81349	RCR07G182JS	1.8K 5% 1/4W Carbon Comp	R19
30	2	81349	RCR07G221JS	220 5% 1/4W Carbon Comp	R19
31	3	81349	RCR07G222JS	2.2K 5% 1/4W Carbon Comp	R5,R35
32	2	81349	RCR07G223JS	22K 5% 1/4W Carbon Comp	R27,R28,R30
33	1	81349	RCR07G390JS	39 ohm 5% 1/4W Carbon Comp	R15
34	1	81349	RCR07G392JS	3.9K 5% 1/4W Carbon Comp	R13
35	4	81349	RCR07G471JS	470 5% 1/4W Carbon Comp	R1,R8-10, R12,R23
36	3	81349	RCR07G472JS	4.7K 5% 1/4W Carbon Comp	R21,R26,R29
37	3	81349	RCR07G511JS	510 5% 1/4W Carbon Comp	R3,R4,R7

ASSEMBLY NUMBER 117240-01 - DIGITAL DELAY GENERATOR A1 (Continued)

ITEM	QTY	MANUFAC-TURER'S CODE	PART NUMBER	DESCRIPTION	REF. DESIG.
38	2	81349	RCR07G821JS	820 ohm 5% 1/4W Carbon Comp	R16,R17,
39	1	81349	RCR07G270JS	27 ohm 5% 1/4W Carbon Comp	R31
40	1	81349	RCR07G104JS	100K ohm 5% 1/4W Carbon Comp	R33
41	1	81349	RCR07G121JS	120 ohm 5% 1/4W Carbon Comp	R34
42	1	81349	RCR42G750JS	75 ohm 5% 2W Carbon Comp	R32
43	1	01295	74LS00N	Quad 2 Input NAND Gate	U5
44	2	01295	74LS04N	Hex Inverter	U1,U4
45	3	01295	74LS30N	Dual 6 Input NAND Gate	U6,U8,U10
46	1	01295	74LS112N	Dual JK	U12
47	1	01295	74LS151N	Multiplexer	U15
48	3	01295	74LS273N	Octal D Flip Flop	U7,U9,U11
49	1	01295	74LS290N	Decade Counter	U19
50	3	01295	74LS390N	Decade Counter	U16,U17,U18
51	1	01295	UA7952CKC	-5.2V Regulator	U24
52	2	34649	P8216	Buss Driver	U2,U3
53	1	04713	MC4044P	Phase Comparator	U13
54	1	04713	MC10102P	Quad 2 Input NAND Gate	U21
55	1	04713	MC10138P	Dual JK	U20
56	1	27014	LM320MP-12	-12V Regulator	U22
57	1	27014	LM342P-12	+12V Regulator	U23
58	1	27014	LM741CN	Op Amp	U14

ASSEMBLY NUMBER 117240-01 - DIGITAL DELAY GENERATOR A1 (Continued)

ITEM	QTY	MANUFAC-TURER'S CODE	PART NUMBER	DESCRIPTION	REF. DESIG.
59	1	01295	C9308-02	8 Pin Socket	
60	8	01295	C9314-02	14 Pin Socket	
61	9	01295	C9316-02	16 Pin Socket	
62	3	01295	C9320-02	20 Pin Socket	
63	2	56289	196D156X-9020K41	15 MFD, 20V, TANT	C27,C29
64	2	56289	196D156X-9035PE4	15 MFD, 35V, TANT	C13,C17

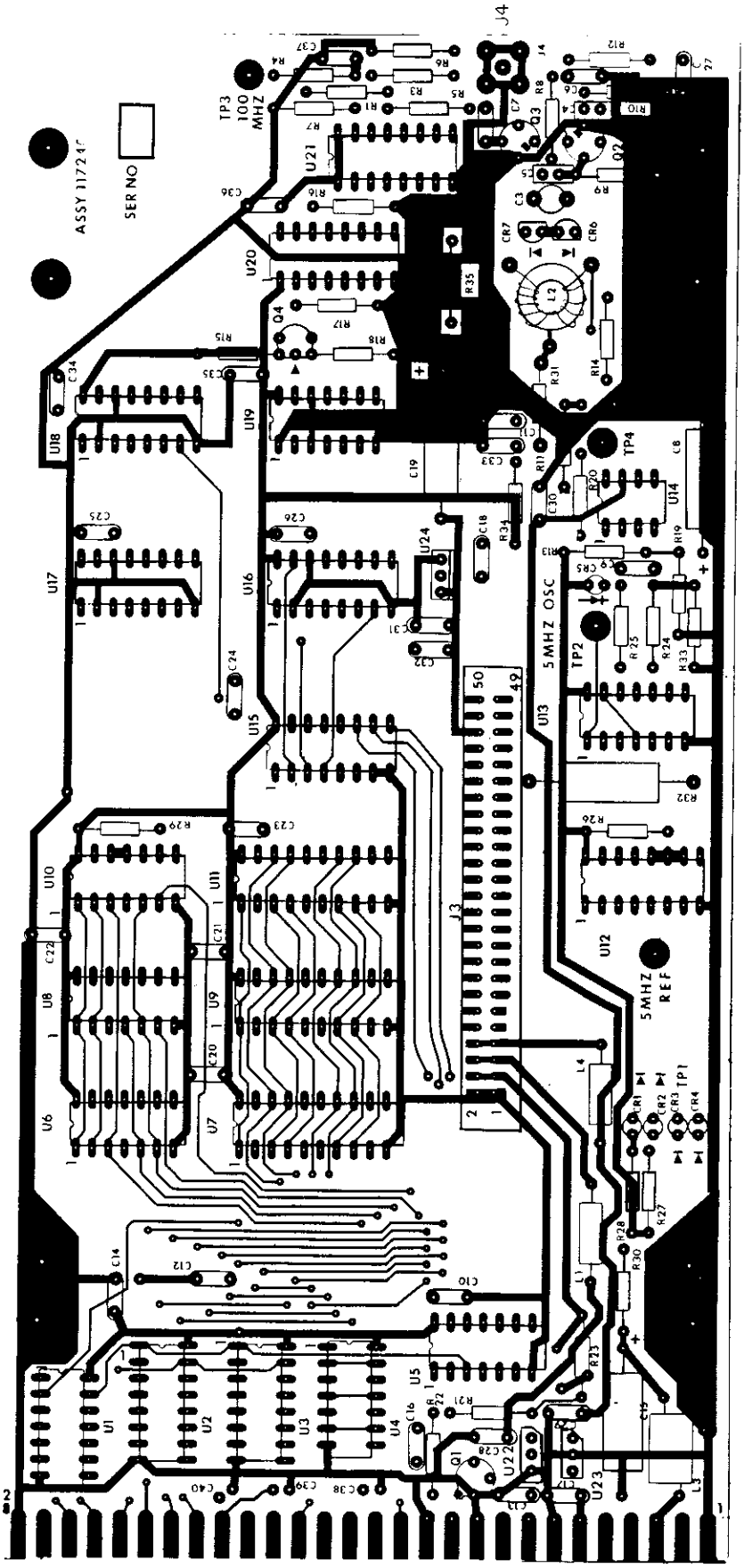

Figure 6.2 AS210-04 Digital Delay Generator Assembly, A1

ASSEMBLY NUMBER 117245-01 - DIGITAL DELAY GENERATOR A2

ITEM	QTY	MANUFAC-TURER'S CODE	PART NUMBER	DESCRIPTION	REF. DESIG.
1	1	33472	117248	PC Board	
2	0	33472	117246	Schematic	
3	0	33472	117245	Assembly Drawing	
4	1	81349	CKO5BX102K	.001 UFD 10% Ceramic Capacitor	C2
5	10	81349	CKO5BX104K	.1UFD 10% Ceramic Capacitor	C6-C10,C12, C14,C17-C25, C28,C30
6	2	81349	CKO5BX272K	2700 PFD 10% Ceramic Capacitor	C3,C4
7	1	81349	CKO5BX100K	10 PFD 10% Ceramic	C5
8	1	81349	CKO5BX471K	470 PFD 10% Ceramic Capacitor	C1
9	2	81349	100-100-CGS339J	3.3 PFD 5% Ceramic Capacitor	C31,C32
10	5	56289	196D156X-9020KA1	15 UFD 10% Solid Tantalum	C15,C16,C26, C27,C29
11	4	04713	1N3064	Diode	CR1,CR4
12	4	15849	2010B-1	Terminal	
13	36	09769	2-331272-6	Minipin	
14	1	53387	3433-2202	50 Pin PC Mount Male Header	J3
15	1	27264	22-03-2251	25 Pin Wafer	J2
16	3	98291	51-051-0000	Snap-On Conhex Connector	J1,J4,J5
17	1	02114	VK200-20/4B	Wide Band Choke	L1
18	7	04713	MPS3639	PNP Transistor	Q1-Q7
19	2	83149	MS51957-4	Screw PNH 2-56 x 5/16	
20	4	81349	NAS620-C2	Reduced OD Flat Washer #2	
21	2	81349	MS35338-134	Split Lock Washer #2	
22	2	81349	NAS671-C2	Small Pattern Hex Nut #2	
23	6	81349	RCR05G820JS	82 ohm 5% 1/8W Carbon Comparator	R70,R71, R82-R85

ASSEMBLY NUMBER 117245-01 - DIGITAL DELAY GENERATOR A2 (Continued)

ITEM	QTY	MANUFAC-TURER'S CODE	PART NUMBER	DESCRIPTION	REF. DESIG.
24	4	81349	RCR05G131JS	130 ohm 5% 1/8W Carbon Comparator	R9,R19,R26, R27
25	5	81349	RCR05G151JS	150 ohm 5% 1/8W Carbon Comparator	R4,R5,R14, R42,R44
26	8	81349	RCR05G181JS	180 ohm 5% 1/8W Carbon Comparator	R7,R30,R32, R35,R38,R49, R61,R72
27	1	81349	RCR05G221JS	220 ohm 5% 1/8W Carbon Comparator	R3
28	8	81349	RCR05G271JS	270 ohm 5% 1/8W Carbon Comparator	R6,R31,R34, R37,R40,R50, R63,R73
29	15	81349	RCR05G301JS	300 ohm 5% 1/8W Carbon Comparator	R1,R2,R18, R68,R69
30	11	81349	RCR05G390JS	39 ohm 5% 1/8W Carbon Comparator	R13,R20,R21, R28,R29,R53, R55,R57,R59, R62,R80
31	3	81349	RCR05G471JS	470 ohm 5% 1/8W Carbon Comparator	R12,R15,R43
32	4	81349	RCR05G472JS	4.7K 5% 1/8W Carbon Comparator	R24,R25,R52, R66
33	7	81349	RCR05G511JS	510 ohm 5% 1/8W Carbon Comparator	R10,R67, R74-R78
34	14	81349	RCR05G821JS	820 ohm 5% 1/8W Carbon Comparator	R8,R11,R33, R36,R39,R41, R45-R48,R51, R64,R79,R81
35	5	81349	RCR05G151JS	150 ohm 5% 1/8W Carbon Comparator	R54,R56,R58, R60,R65
36	2	81349	RN55C2671FM	2670 ohm 1% 1/4W, Metal Film	R16,R22
37	2	73139	82-PAR-2K	2K Variable Resistor	R17,R23
38	1	75378	750-61-R680	Resistor, Network	U6
39	3	75378	750-81-R820	Resistor, Network	U1,U9,U21

ASSEMBLY NUMBER 117245-01 - DIGITAL DELAY GENERATOR A2 (Continued)

ITEM	QTY	MANUFAC-TURER'S CODE	PART NUMBER	DESCRIPTION	REF. DESIG.
40	1	01295	74LS00N	Quad 2 Input NAND Gate	U23
41	2	01295	74LS04N	Hex Inverter	U10,U35
42	1	01295	74LS20N	Triple 4 Input NAND Gate	U30
43	1	01295	74LS112N	Dual JK	U36
44	8	01295	74LS151N	Multiplexer	U12,U14,U25, U26,U27,U37, U38,U39
45	4	01295	74LS190N	Decade Counter	U31,U32,U33, U34
46	1	01295	74LS290N	Decade Counter	U24
47	2	01295	74LS390N	Decade Counter	U11,U13
48	1	04713	MC01231P	Dual D Hi-Speed FF	U3
49	1	04713	MC1678P	Decade Counter	U20
50	2	04713	MC10102P	Quad 2 Input NAND Gate	U4,U22
51	2	04713	MC12009P	Triple 4 Input NAND Gate	U5,U18
52	2	04713	MC10131P	Dual D Flip Flop	U7,U16
53	1	04713	MC10135P	Dual JK	U2
54	1	04713	MC10138P	Decade Counter	U8
55	3	04713	MC10198P	One Shot	U15,U17,U19
56	2	33472	117190	Pulse Amplifier	U28,U29
57	1	13103	6007A	Heat Sink, with Cap.	
58	3	13103	6011B	Heat Sink	
59	5	01295	C9314-02	14 Pin Socket	
60	27	01295	C9316-02	16 Pin Socket	